FERROELECTRIC MEMORY DEVICES

Abstract of the Disclosure

In the present invention, ferroelectric memory devices using a ferroelectric planarization layer and methods of fabricating the same are disclosed. According to the method of the present invention, a conductive layer is formed on an interlayer insulation layer having a contact plug and patterned to form capacitor bottom electrode patterns. A ferroelectric layer for planarization is formed to fill a space between the bottom electrode patterns, and then another ferroelectric layer for a capacitor is formed on the bottom electrode pattern and the ferroelectric layer for planarization.